

Winter Semester 2024-2025

MVLD505P – ASIC Design

SLOT: L23+L24

Submitted to School of Electronics Engineering

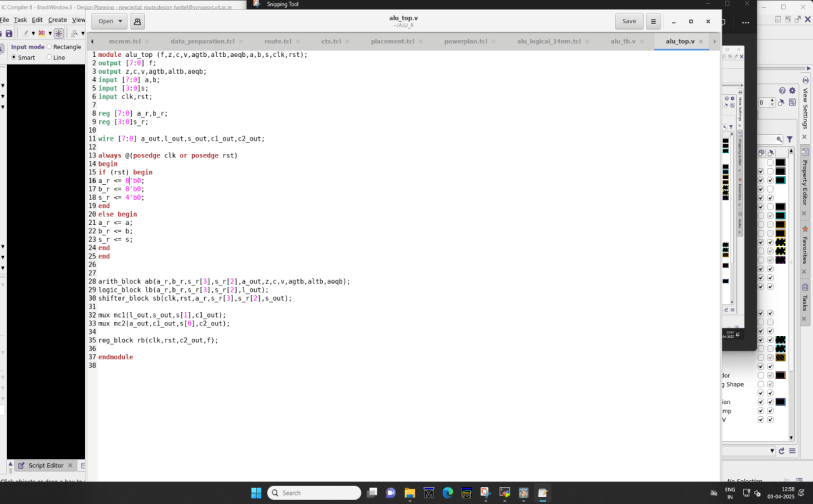
Submitted by:

Name: CJ kiran

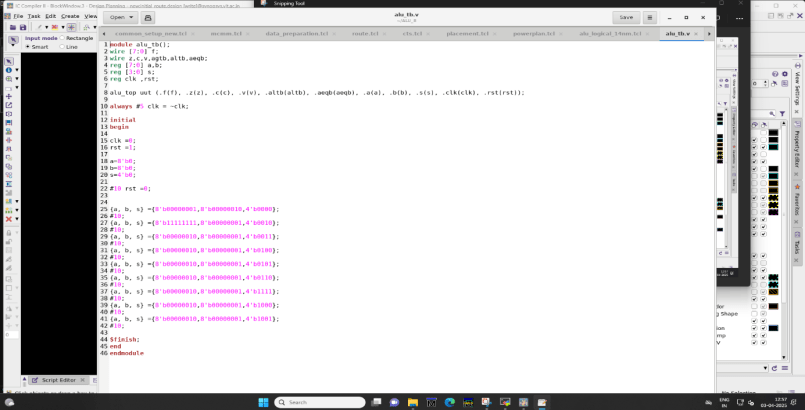
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**TASK 5:- ASIC Physical Design Flow**- **placement determines cell locations, CTS (Clock Tree Synthesis) optimizes clock distribution, and routing**

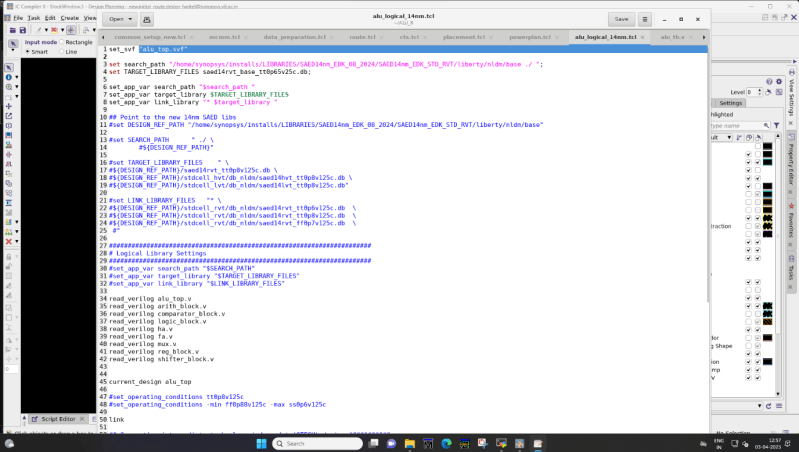
**ALU Verilog code**



**ALU\_TB.V**



**Netlist for ALU**

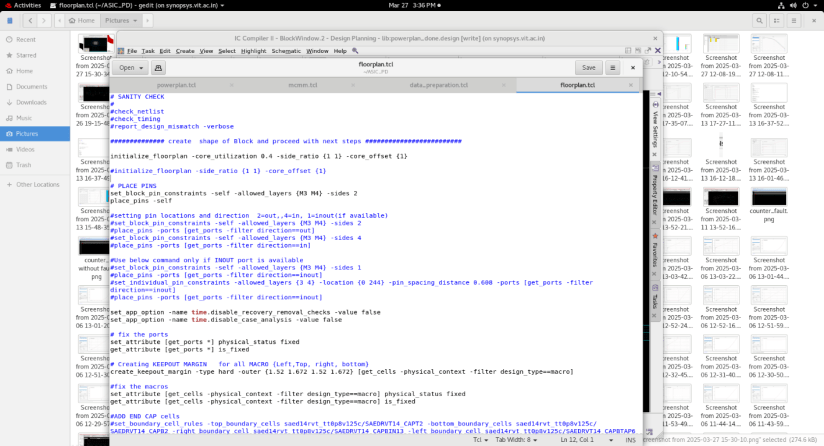
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**Phase -1 ASIC Physical Design Flow**,- **Floorplanning and Power Planning**

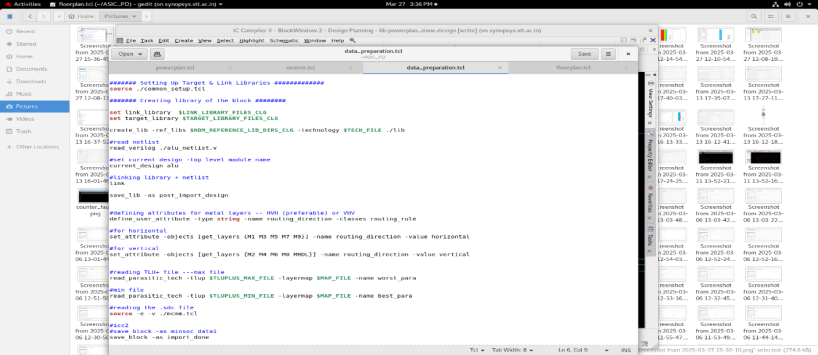
In the **ASIC Physical Design Flow**, **Floorplanning and Power Planning** are crucial steps that significantly impact the chip’s performance, power efficiency, and manufacturability. These steps define the **physical arrangement of components**, ensure optimal connectivity, and establish a robust **power distribution network** to prevent power-related issues.

perform **Floorplanning and Power Planning** using **Synopsys IC Compiler II**.

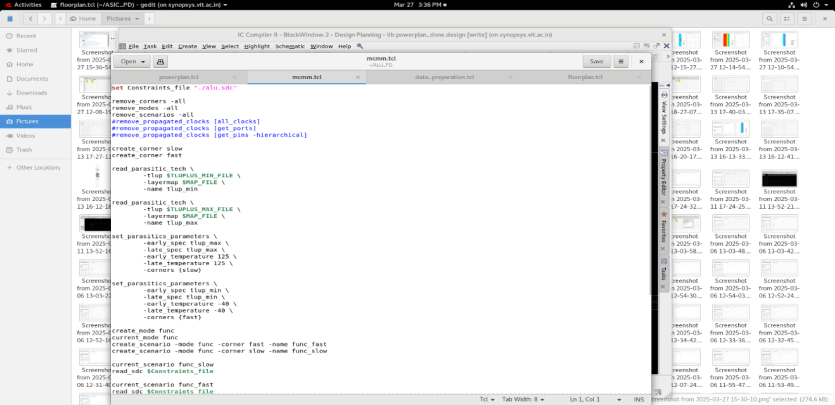
**Floorplan.tcl**



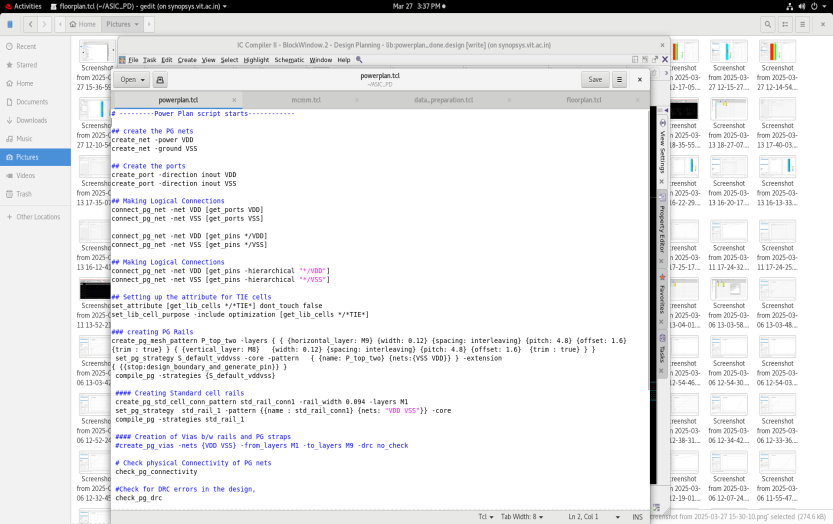
**Data\_preparation.tcl**



**MCMM.tcl- MCMM (Multi-Corner Multi-Mode) Analysis**



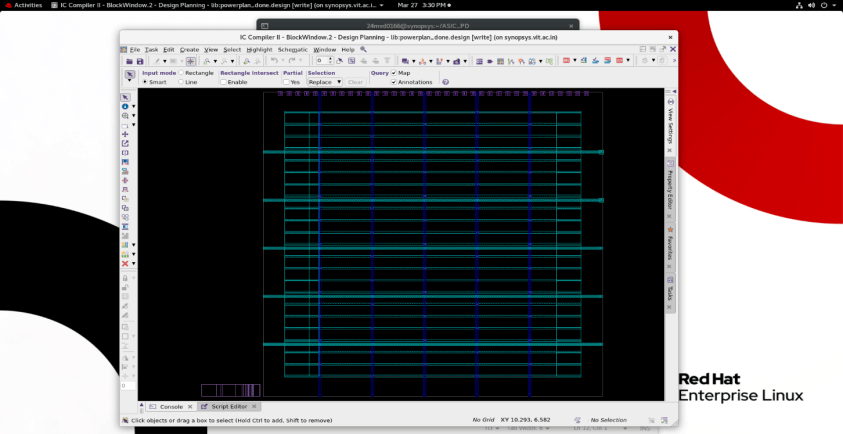
**Powerplan.tcl**



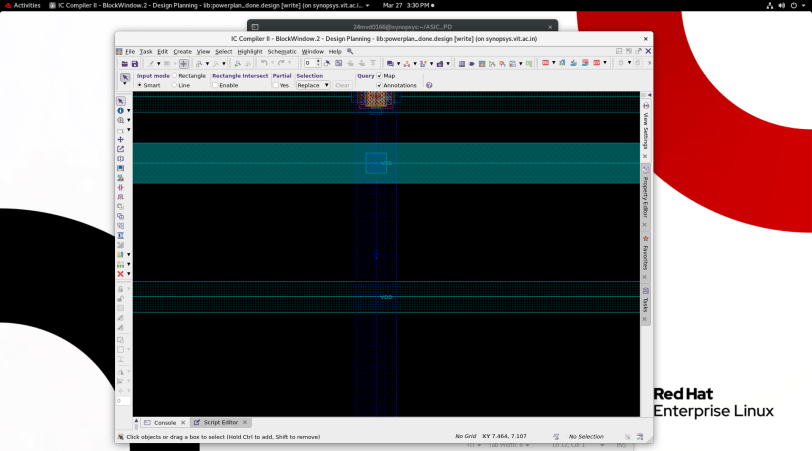
**Standard Cells-** Standard cells are pre-designed logic gates,(ALU block) used to build an ASIC. They are placed in rows inside the core area and connected during placement and routing.



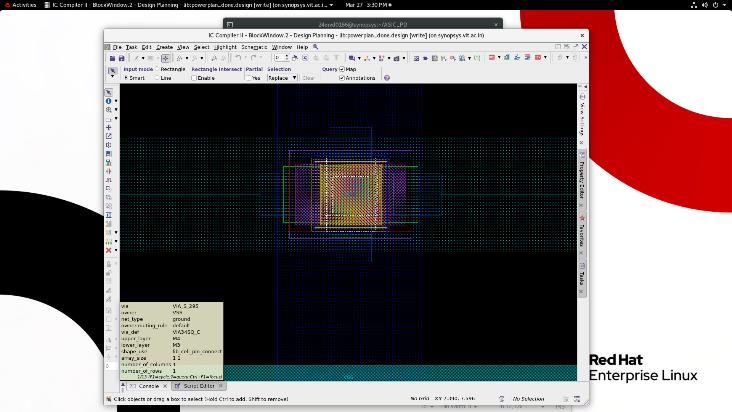
**Floorplan**



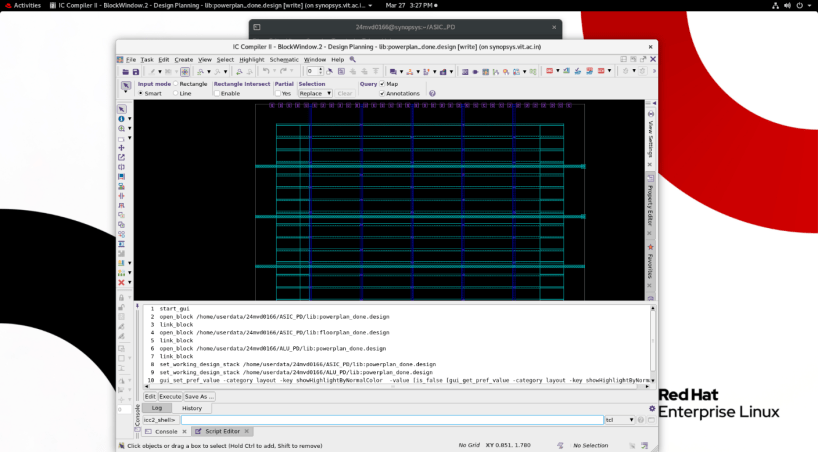
**VSS and VDD**



**Via Block shows the vss and vdd paths**



**Floorplanning and Power Planning- log**



**Phase 2- Placement determines cell locations, CTS (Clock Tree Synthesis) optimizes clock distribution, and routing**

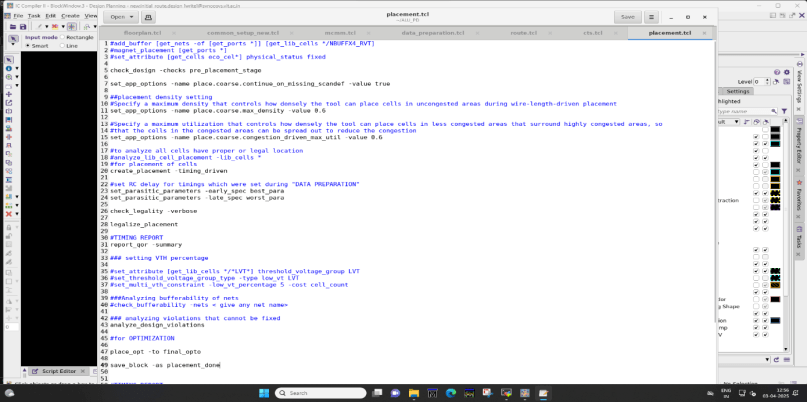
In ASIC Physical Design, achieving a high-performance and manufacturable chip requires precise execution of Placement, Clock Tree Synthesis (CTS), and Routing. These steps are performed using Synopsys IC Compiler II (ICC2), a leading place-and-route (PnR) tool used in advanced semiconductor design.

**Overview of the Stages**

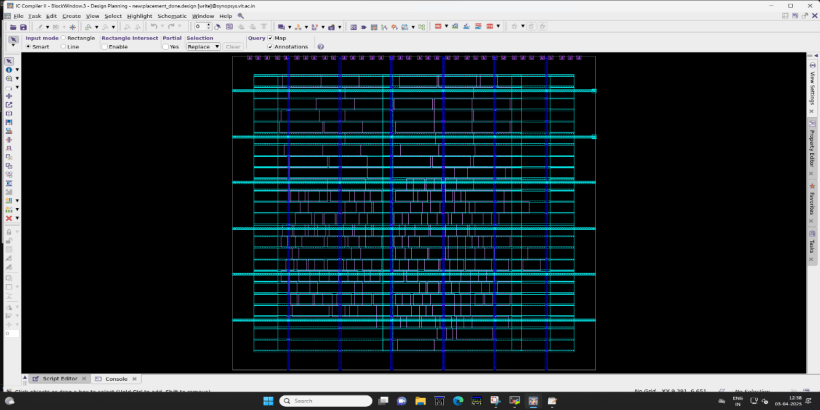
**Placement**: Determines the physical locations of standard cells and macros to optimize timing, power, and congestion.  
 Clock Tree Synthesis (CTS): Builds a balanced clock distribution network, minimizing clock skew and latency.  
 **Routing**: Establishes metal interconnections between components while ensuring signal integrity and manufacturability.

These steps play a critical role in achieving timing closure, power efficiency, and design rule compliance, making them fundamental to the ASIC design flow

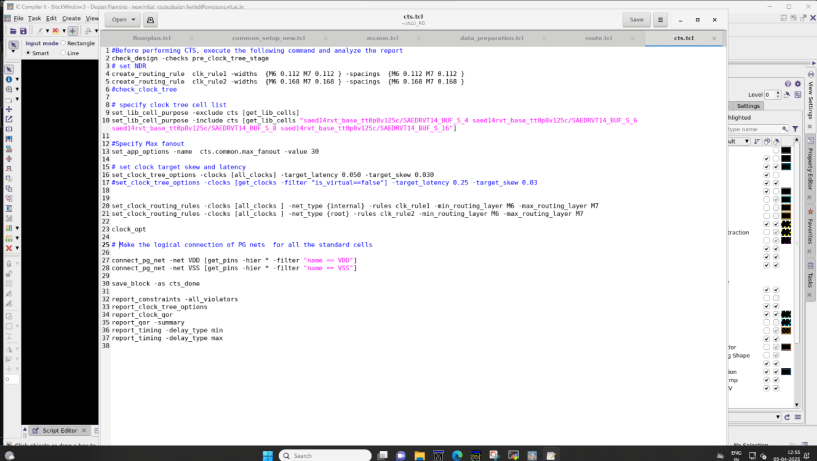
Placement.tcl

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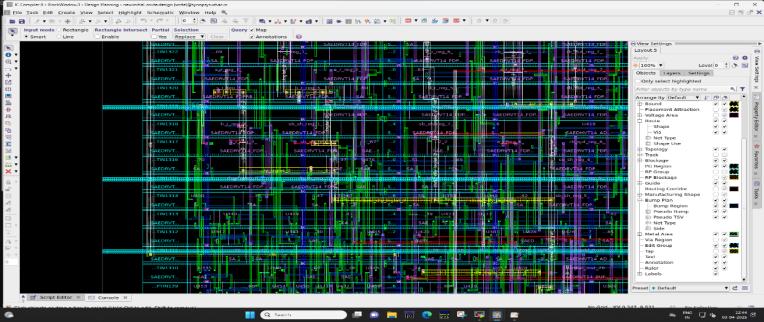
**Placement**

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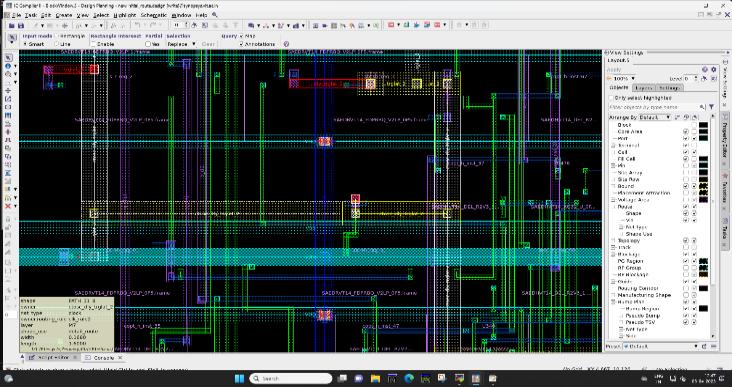
**CTS (Clock Tree Synthesis).tcl**

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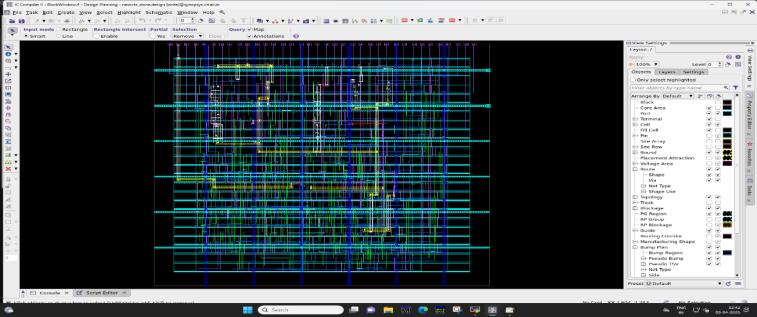
**Clock path**

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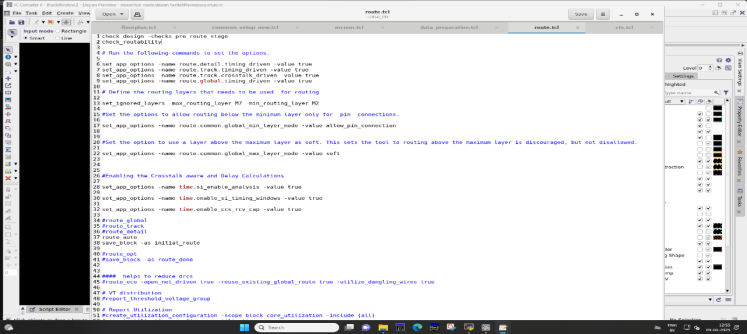
**Clock paths -green lines is cts**

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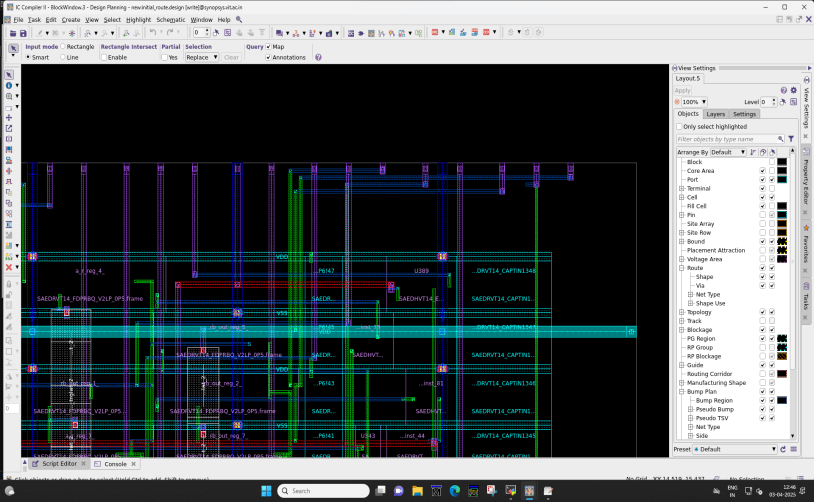
**Final clock path**

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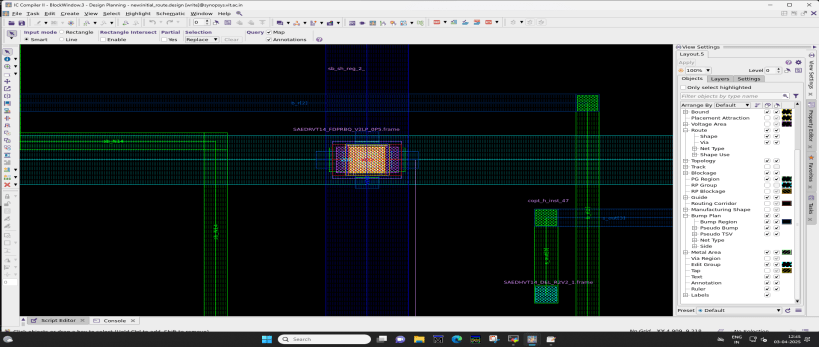
**Routing.tcl**

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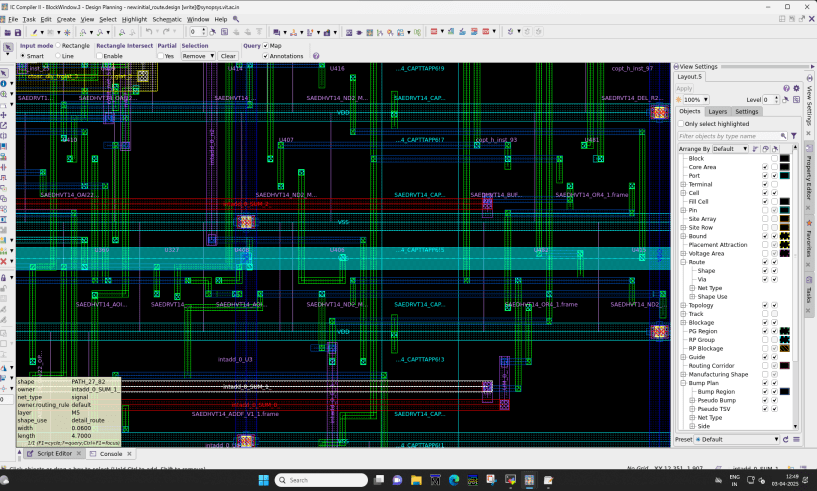
**Routing paths**

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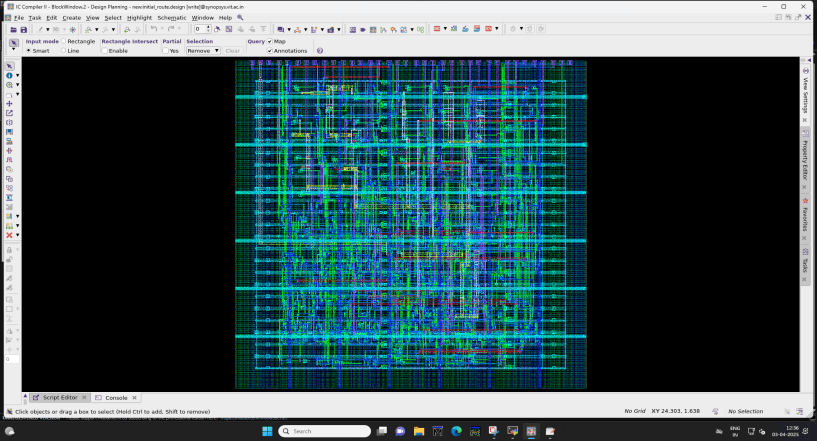
**Via paths**

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**Power lines -red lines**

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**Final output – After doing Placement determines cell locations, CTS (Clock Tree Synthesis) optimizes clock distribution, and routing**

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**Conclusion**

**ASIC Physical Design Flow**

The ASIC Physical Design Flow involves multiple critical stages to transform a synthesized netlist into a manufacturable layout while ensuring optimal performance, power, and area (PPA). The key phases include

**Floor planning and Power Planning**

* Organizes macros and standard cells to optimize area, reduce congestion, and improve timing.
* Establishes a robust power distribution network (PDN) to prevent IR drop and electromigration issues.

**Placement**

* Determines the optimal locations for standard cells and macros to minimize wirelength and improve timing.
* Ensures congestion-free placement while maintaining power and signal integrity.

**Clock Tree Synthesis (CTS)**

* Distributes the clock signal efficiently to reduce clock skew and latency.
* Uses buffers and inverters to balance the clock network for optimal timing performance.

**Routing**

* Establishes metal interconnections between components while ensuring minimal delays and DRC (Design Rule Check) compliance.
* Finalizes the design for signoff and fabrication by optimizing signal integrity and manufacturability.

Each of these steps is essential in achieving a high-performance, low-power, and manufacturable ASIC design. Proper execution ensures that the final chip meets timing, power, and area constraints, making it ready for signoff and tape-out.